In the Claims:

1. (Previously Presented) A semiconductor device, comprising:

a workpiece;

a first insulating layer formed over the workpiece;

at least one second insulating layer formed over the first insulating layer; and

a plurality of metal-insulator-metal (MIM) capacitors formed in the first insulating layer and the at least one second insulating layer, at least one of the plurality of MIM capacitors comprising a first conductive layer, a dielectric layer disposed over the first conductive layer, and a second conductive layer formed over the dielectric layer, and wherein the first conductive layer extends completely to a top surface of the at least one second insulating layer, wherein the at least one second insulating layer comprises a recessed region between at least two adjacent MIM capacitors, the at least two adjacent MIM capacitors having top plates comprised of the second conductive layer, wherein the second conductive layer within the recessed region electrically couples the top plates of the at least two adjacent MIM capacitors.

2. (Previously Presented) The semiconductor device according to Claim 1, wherein the first conductive layer and the second conductive layer comprise a refractory metal, TiN, TaN, Ta, TaSiN, TiW, NiCr, MoN, Ru, WN, WSi, Cu, Al, W, Ti, Ta, Co, N, Ni, Mo, other metals, combinations thereof, or polysilicon, and wherein the MIM capacitors are formed in an interconnect layer of the semiconductor device.

3. (Original) The semiconductor device according to Claim 1, wherein the dielectric layer comprises Al, Si, O, N, Ti, Ta, lead-zirconate-titanate (PZT), barium strontium titanate (BST), Ta_2O_5, Al_2O_3, SiO_2, or combinations thereof.

4. (Previously Presented) The semiconductor device according to Claim 1, wherein the at least one second insulating layer comprises 2, 3, 4, 5, or 6 or more insulating layers, wherein the MIM capacitors are formed in the entire thicknesses of the second insulating layers.

5. (Previously Presented) The semiconductor device according to Claim 4, wherein the workpiece comprises a plurality of elements formed therein, further comprising:

at least one third insulating layer disposed between the workpiece and the first insulating layer; and

at least one conductive region formed in each third insulating layer abutting the first conductive layer of at least one of the plurality of MIM capacitors, wherein each conductive region and the first conductive layer comprise a bottom plate of at least one of the plurality of MIM capacitors, and wherein the at least one conductive region makes electrical contact to an element in the workpiece.

6. (Previously Presented) The semiconductor device according to Claim 5, wherein the at least one third insulating layer comprises a first metallization layer of the semiconductor device, wherein the first insulating layer comprises a first via layer of the semiconductor device, wherein the at least one second insulating layer comprises a second metallization layer of the semiconductor device, and wherein at least one of the

plurality of MIM capacitors is formed in the first via layer and the second insulating layer of the semiconductor device.

7. (Previously Presented) A semiconductor device, comprising:

a workpiece;

a first insulating layer formed over the workpiece;

at least one second insulating layer formed over the first insulating layer; and

at least one metal-insulator-metal (MIM) capacitor formed in the first insulating layer and the at least one second insulating layer, the at least one MIM capacitor comprising a first conductive layer, a dielectric layer disposed over the first conductive layer, and a second conductive layer formed over the dielectric layer, and wherein the first conductive layer extends completely to a top surface of the at least one second insulating layer;

wherein the at least one second insulating layer comprises 2, 3, 4, 5, or 6 or more insulating layers, wherein the at least one MIM capacitor is formed in the entire thicknesses of the second insulating layers;

wherein the workpiece comprises a plurality of elements formed therein, further comprising at least one third insulating layer disposed between the workpiece and the first insulating layer and at least one conductive region formed in each third insulating layer abutting the first conductive layer of the at least one MIM capacitor, wherein each conductive region and the first conductive layer comprise a bottom plate of the at least one MIM capacitor, and wherein the at least one conductive region makes electrical contact to an element in the workpiece; and

wherein the at least one third insulating layer comprises a first metallization layer, at least one first via layer and at least one second metallization layer of the semiconductor device, wherein the first insulating layer comprises at least one second via layer of the semiconductor device, wherein the at least one second insulating layer comprises at least one third metallization layer of the semiconductor device, wherein the at least one MIM capacitor is formed in the at least one second via layer and the at least one third insulating layer of the semiconductor device, and wherein a bottom plate of the at least one MIM capacitor comprises the first conductive layer and the conductive regions in the third insulating layer.

8. (Previously Presented) The semiconductor device according to Claim 1, wherein at least one of the plurality of MIM capacitors comprises an array of memory devices, the array having a dimension of 2x1 or greater.

9. (Original) The semiconductor device according to Claim 1, wherein the first conductive layer comprises a bottom electrode, the dielectric layer comprises a capacitor dielectric, and the second conductive layer comprises a top electrode, wherein the bottom electrode, top electrode, or both are formed by a chemical-mechanical polish (CMP) process.

10. (Previously Presented) The semiconductor device according to Claim 1, wherein the MIM capacitors are formed in a stand-alone memory device, embedded memory device, non-voltage memory device, ferro-electro memory device, magneto-electro memory device, static random access memory (SRAM) device, dynamic random access

memory (DRAM) device, digital device, RF device, analog device, or mixed-mode device.

11. (Previously Presented) The semiconductor device according to Claim 1, wherein the workpiece comprises a first region and a second region, wherein at least one of the plurality of MIM capacitors is formed over the first region, further comprising conductive regions formed in the first insulating layer and the at least one second insulating layer over the second region of the workpiece.

12. (Previously Presented) A semiconductor device, comprising:

a workpiece;

a first insulating layer formed over the workpiece;

at least one second insulating layer formed over the first insulating layer; and

at least one metal-insulator-metal (MIM) capacitor formed in the first insulating layer and the at least one second insulating layer, the at least one MIM capacitor comprising a first conductive layer, a dielectric layer disposed over the first conductive layer, and a second conductive layer formed over the dielectric layer, and wherein the first conductive layer extends completely to a top surface of the at least one second insulating layer;

wherein the workpiece comprises a first region and a second region, wherein the at least one MIM capacitor is formed over the first region, further comprising conductive regions formed in the first insulating layer and the at least one second insulating layer over the second region of the workpiece; and

wherein the first region comprises a DRAM region, wherein the second region

comprises a logic region, and wherein the at least one MIM capacitor comprises a storage node of a DRAM memory cell in the DRAM region.

13. (Previously Presented) A semiconductor device, comprising:

a workpiece;

a first insulating layer formed over the workpiece;

at least one second insulating layer formed over the first insulating layer; and

at least one metal-insulator-metal (MIM) capacitor formed in the first insulating layer and the at least one second insulating layer, the at least one MIM capacitor comprising a first conductive layer, a dielectric layer disposed over the first conductive layer, and a second conductive layer formed over the dielectric layer, and wherein the first conductive layer extends completely to a top surface of the at least one second insulating layer;

wherein the workpiece comprises a first region and a second region, wherein the at least one MIM capacitor is formed over the first region, further comprising conductive regions formed in the first insulating layer and the second insulating layer over the second region of the workpiece; and

wherein the first insulating layer comprises a via layer of the semiconductor device, wherein the second insulating layer comprises a metallization layer of the semiconductor device, and wherein the conductive regions in the second region comprise a dual damascene structure.

14. (Cancelled)

15. (Currently Amended) The semiconductor device according to Claim 1, wherein the workpiece comprises a plurality of elements formed therein, further comprising a third insulating layer formed between the workpiece and the first insulating layer, further comprising at least one first conductive region disposed in the third insulating layer abutting the first conductive layer of the at least one of the plurality of MIM ~~capacitor,~~ capacitors, wherein the at least one first conductive region and the first conductive layer comprise a bottom plate of at least one of the plurality of MIM capacitors.

16. (Original) The semiconductor device according to Claim 15, wherein the at least one first conductive region comprises a conductive barrier layer and a conductive material disposed over the conductive barrier layer.

17. (Previously Presented) The semiconductor device according to Claim 15, wherein the at least one first conductive region electrically couples at least one of the plurality of MIM capacitors to an element in the workpiece.

18. (Currently Amended) The semiconductor device according to Claim 15, wherein the [[st]] at least one first conductive region and the third insulating layer comprise a first metallization layer of the semiconductor device, wherein the first insulating layer comprises a first via layer of the semiconductor device, wherein the second insulating layer comprises a second metallization layer of the semiconductor device, and wherein at least one of the plurality of MIM capacitors is formed in the first via layer and the second metallization layer of the semiconductor device.

19. (Previously Presented) A semiconductor device, comprising:

a workpiece;

a first insulating layer formed over the workpiece;

at least one second insulating layer formed over the first insulating layer; and

at least one metal-insulator-metal (MIM) capacitor formed in the first insulating layer and the at least one second insulating layer, the at least one MIM capacitor comprising a first conductive layer, a dielectric layer disposed over the first conductive layer, and a second conductive layer formed over the dielectric layer, and wherein the first conductive layer extends completely to a top surface of the at least one second insulating layer;

wherein the workpiece comprises a plurality of elements formed therein, further comprising a third insulating layer formed between the workpiece and the first insulating layer, further comprising at least one first conductive region disposed in the third insulating layer abutting the first conductive layer of the at least one MIM capacitor, wherein the at least one first conductive region and the first conductive layer comprise a bottom plate of the at least one MIM capacitor; and

further comprising at least one fourth insulating layer disposed between the first insulating layer and the third insulating layer, and a second conductive region formed in each at least one fourth insulating layer between the first conductive region and the at least one MIM capacitor, wherein the second conductive region electrically couples the at least one MIM capacitor to the first conductive region.

20. (Previously Presented) The semiconductor device according to Claim 19, wherein the third insulating layer and the at least one first conductive region comprise a first metallization layer of the semiconductor device, wherein the at least one fourth insulating layer and the second conductive region comprise a first via layer and a second metallization layer of the semiconductor device, wherein the first insulating layer comprises a second via layer of the semiconductor device, wherein the second insulating layer comprises a third metallization layer of the semiconductor device, and wherein the at least one MIM capacitor is formed in the second via layer and the third metallization layer of the semiconductor device.

21. (Previously Presented) The semiconductor device according to Claim 1, wherein the second conductive layer of the plurality of MIM capacitors comprises a conductive barrier layer and a conductive material disposed over the conductive barrier layer.

22. (Previously Presented) A semiconductor device, comprising:

a workpiece;

a first insulating layer formed over the workpiece;

a second insulating layer formed over the first insulating layer;

at least one third insulating layer formed over the second insulating layer; and

a plurality of metal-insulator-metal (MIM) capacitors formed in the at least one third insulating layer, the second insulating layer, and the first insulating layer, at least one of the plurality of MIM capacitors comprising a first conductive layer, a dielectric layer disposed over the first conductive layer, and a second conductive layer formed over the dielectric layer, wherein the at least one third insulating layer comprises a recessed

region between at least two adjacent MIM capacitors, the at least two adjacent MIM capacitors having top plates comprised of the second conductive layer, wherein the second conductive layer within the recessed region electrically couples the top plates of the at least two adjacent MIM capacitors.

23. (Previously Presented) The semiconductor device according to Claim 22, wherein the first insulating layer comprises a first via layer of the semiconductor device, wherein the second insulating layer comprises a first metallization layer of the semiconductor device, wherein the at least one third insulating layer comprises at least one second via layer and at least one second metallization layer of the semiconductor device, wherein at least one of the plurality of MIM capacitors extends through the entire thicknesses of the first via layer, the first metallization layer, the at least one second via layer, and the at least one second metallization layer.

24. (Previously Presented) The semiconductor device according to Claim 22, wherein the workpiece comprises a plurality of elements formed therein, further comprising:

at least one fourth insulating layer disposed between the workpiece and the first insulating layer; and

at least one conductive region formed in each fourth insulating layer between the first conductive layer of at least one of the plurality of MIM capacitors and an element in the workpiece, wherein each conductive region and the first conductive layer comprise a bottom plate of at least one of the plurality of MIM capacitors.

25. (Previously Presented) The semiconductor device according to Claim 24, wherein the at least one fourth insulating layer comprises a first metallization layer of the semiconductor device, wherein the first insulating layer comprises a first via layer of the semiconductor device, wherein the second insulating layer comprises a second metallization layer of the semiconductor device, wherein the at least one third insulating layer comprises at least one second via layer and at least one third metallization layer of the semiconductor device, and wherein at least one of the plurality of MIM capacitors extends through the entire thicknesses of the first via layer, the second metallization layer, the at least one second via layer, and the at least one second metallization layer.

26. (Cancelled)

27. (Previously Presented) A semiconductor device, comprising:

a workpiece;

at least one first insulating layer formed over the workpiece; and

a plurality of metal-insulator-metal (MIM) capacitors formed in the at least one first insulating layer, the plurality of MIM capacitors comprising a first conductive layer, a dielectric layer disposed over the first conductive layer, and a second conductive layer formed over the dielectric layer, the second conductive layer comprising a top plate of the plurality of MIM capacitors, wherein a top of the at least one first insulating layer comprises a recessed region between at least two adjacent MIM capacitors, and wherein the second conductive layer fills the recessed region of the top of the at least one first insulating layer, electrically coupling together the top plates of the at least two adjacent MIM capacitors.

28. (Original) The semiconductor device according to Claim 27, wherein the at least one first insulating layer comprises at least two insulating layers, wherein one first insulating layer comprises a via layer of the semiconductor device, and wherein another first insulating layer comprises an interconnect layer formed over the via layer.

29. (Previously Presented) The semiconductor device according to Claim 27, wherein the workpiece comprises a plurality of elements formed therein, further comprising at least one second insulating layer formed between the workpiece and the first insulating layer, further comprising a conductive region formed in each at least one second insulating layer, the conductive regions electrically coupling the first conductive layer of the MIM capacitors to an element in the workpiece, wherein the conductive regions and the first conductive layer comprise a bottom plate of at least one MIM capacitor.

30. (Currently Amended) The semiconductor device according to Claim 29, wherein the at least one first insulating layer comprises at least two insulating layers, wherein the conductive region and the at least one ~~third~~ second insulating layer comprise at least one first metallization layer of the semiconductor device, wherein one first insulating layer comprises a first via layer formed over the at least one first metallization layer, and wherein another first insulating layer comprises a second metallization layer formed over the first via layer.

31-44. Cancelled

45. (New) The semiconductor device according to Claim 12, wherein a surface of the conductive regions formed in the at least one second insulating layer over the second region of the workpiece and a surface of the second conductive layer over the first region have been polished simultaneously using a chemical mechanical polishing process such that the surface of the conductive regions and the surface of the second conductive layer are substantially coplanar.

46. (New) The semiconductor device according to Claim 12, wherein the conductive regions formed in the at least one second insulating layer over the second region of the workpiece comprise the same material as at least a portion of the second conductive layer over the first region.